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J Shen, JA Abraham - Journal of Electronic Testing, 2000 - Springer
... abstract tests and the tool **Genesys** [25] to **...** environment, in the form of **processor** assembly programs **...** mapping between different levels of **simulation**, mapping low **...**
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... be precise, 2.384 * 1011) SRTL **simulation** cycles of **...** silicon **validation**, the Pentium® 4 **processor** was highly **...** for Microprocessors Using the **Genesys** Test-Program **...**
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[PDF] A generic system **simulator** with novel on-chip cache and throughput models for gigascale ...
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... 2.2.1 Stanford University System Performance **Simulator** (SUSPENS)....13 **...** AREAS WITH THE ARE PREDICTED BY **GENESYS**. **...** DETAILS OF EACH **PROCESSOR** ' S CACHE ARE **...**
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... targeted architecture, and a behavioral **simulator** which is **...** expected values of the various **processor** resources at **... Genesys** tests are therefore not self-checking **...**
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[PDF] Fast Construction of Test Program Generators for Digital Signal Processors
S Rubin, M Levinger, RR Pratt, WP Moore - IEEE INTERNATIONAL CONFERENCE ON ..., 1999 - Citeseer
... the **simulator ...** A Aharon, "Model Based Test Generation for **Processor** Verification" IBM **...** 3. L. Fournier, "**Genesys**-X86: An Automatic Test-Program Generator **...**
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SM Chai, TM Taha, DS Wills, JD Meindl - IEEE Transactions on Very Large Scale Integration(..., 2000 - Citeseer
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S Lo - APPLIED MICROWAVE AND WIRELESS, 2000 - dev.impello.com
... accurate, EM simulations consume considerably more CPU time. ... speed and flexibility of a linear **simulator** such as the one included in the **GENESYS** 7 software ...
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P Paulin, RD Central - Proc. of the EuroMicro, 2000 - iuma.ulpgc.es
... Executable specifications, system **validation** DO THE RIGHT THING ... RISC ASIP Physical **simulation** VLIW Geometry calculation VLIW ... Shading ASIP I/O **processor** H/W ...
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1. Multicore DSP device having **shared** program **memory** with conditional ...

When **processor** core **memory** accesses to internal **memory conflict** with DMA controller **... Register write** module 37 operates to store information in **registers** 38. **...** Functional **verification** of DSP device 100 and debugging of software **...**
www.patentstorm.us/patents/6895479/description.html - Similar

2. Dual read/**write register** file **memory** - US Patent 4933909 Description

Many processing units are required to **share** scratch pad memories. **....** The **register** file **memory** 10 further includes the comparison circuits of **....** It is assumed that the **compare** circuits of block 10-14 have detected no **conflict** and have **...** This can provide a quick way of **verifying** the operation of the **register ...**
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3. Method of comparison between cache and data **register** for non ...

Feb 3, 2009 **...** 5715426, Set-associative cache **memory** with **shared** sense amplifiers **....** RAM refers to read and **write memory**; that is, you can both **write** data into RAM and **....** Data comparison is used during the **verification** portion of this erase **...** a data bit mis-match upon the common line without signal **conflict**. **...**
www.freepatentsonline.com/7486530.html - Similar
by H Hartono - 2009 - Related articles - All 4 versions

4. **VERIFICATION** OF **MEMORY** CONSISTENCY AND TRANSACTIONAL **MEMORY** - Patent

In **shared memory** architectures, a **memory** consistency model typically specifies the **.....** The load results may be buffered (e.g., in **processor**

registers) and flushed to **...** cache flush or pipeline flush instructions, **compare** and swap (CAS) **....** Since VTSO-**conflict** provides an additional level of detail (total **write ...**
www.faqs.org/patents/app/20080288834 - Cached - Similar

5. Complexity alters **verification** strategy

Sep 26, 2001 **...** At first, data read-**write** access from PPC750 to **memory** card and DMA data transfer between host **...** Then simultaneous accesses to **shared memory** by the PPC750 and the host system were performed to **memory** card for verify **conflict** condition. **...** The fact that the NEC team was able to run a 24-**processor**, **...**
www.design-reuse.com/.../complexity-alters-**verification**-strategy.html - Cached - Similar

6. NAS Integer sort on multi-threaded **shared memory** machines

This key generation and a final **verification** step, which **... writing**, the re-design of an earlier 4-**processor** prototype [4] has been completed. **.....** E-**registers** can be accessed by the user to trigger **shared memory** accesses. In **...** date **shared** data structures **conflict**-free, These two properties lead to a perfor- **...**
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by T Grün - Related articles

7. Design and implementation of dual **processor** block with **shared** external

tation of the **processor** board with **shared** cache **memory** is **....** There can be an access **conflict** on a **shared** cache because **.... Write** Miss: A **processor's** request is transferred to the **... Verification** of this design is done with the Cadence CAD **...** many **registers**, a complex control logic with few **registers**, **...**
linkinghub.elsevier.com/retrieve/pii/S0141933196011222 - Similar
by SW Kim - 1997 - Related articles

8. Integrated **Verification** Approach during ADL-driven **Processor** Design

the same set of test-cases, and **compare** the **processor** states in each cycle, as obtained in them. **....** static analysis of a LISA model, we derive a global **conflict** graph, **...** if more than one enable **write memory** signal is high at the **...** Here, the the ADL description of **register write** access and **...**
doi.ieeecomputersociety.org/10.1109/RSP.2006.21 - Similar
by A Chattopadhyay - All 4 versions

9. [PS] Decoupled Hardware Support for Distributed **Shared Memory**

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We **compare** the performance of the two decoupled systems **....** does not **conflict** with the tag, the device allows the **memory** con-. troller to respond. **... write** to the block will cause the **processor** to initiate an invalida- **.....** detailed enough that they were used for initial design

verification ...
ftp://ftp.cs.wisc.edu/wwt/isca96_dcpld.ps - Similar
by SK Reinhardt - Cited by 81 - Related articles - All 16 versions

10. silicon hive Technology

The **processor** needs to resolve this **conflict** by selecting alternate routing **...** Moreover, the number of **register** and **memory** accesses can be reduced by providing **...** internal **register** bandwidth to read and **write** operands from and to. **....** rather than large unified **register** files and centrally **shared** memories that **...**
www.siliconhive.com/Flex/Site/Page.aspx?PageID=13284 - Cached - Similar

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... for system-on-a-chip by using a C/C++ simulator and FPGA emulator with **shared register** ...- psu.edu [PDF]
Y Nakamura, K Hosokawa, I Kuroda, K ... - Proceedings of the 41st annual conference on Design ..., 2004 - portal.acm.org
... and a simulator, to model and **simulate** SoCs **...** G. Mas, G. Barrett, and C. Berthet, "Functional **verification** methodology of Chameleon **processor**", Proceedings of **...**
Cited by 39 - Related articles - BL Direct - All 14 versions

[PDF] Genesys-pro: Innovations in **test** program generation for functional **processor verification**
A Adir, E Almog, L Fournier, E Marcus, M ... - IEEE Design & **Test** of Computers, 2004 - cs.bris.ac.uk
... a large set of **verification** events, there **...** separate instruction sequences for each **processor** or thread **...** architecture reference model for **simulating** the generated **...**
Cited by 46 - Related articles - View as HTML - BL Direct - All 8 versions

Industrial experience with **test** generation languages for **processor verification**- dac.com [PDF]
M Behm, J Ludden, Y Lichtenstein, M Rimon, ... - Proceedings of the 41st annual conference on Design ..., 2004 - portal.acm.org
... templates takes 90 days to **simulate**, while the **...** into IBM's **test** generator for **processor verification** had two **...** is several changes in the **verification** method- ology **...**
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Parallel discrete event simulation using **shared memory**- uoregon.edu [PDF]
D Reed, AD Malony, BD McCredie - IEEE Transactions on Software Engineering, 1988 - doi.ieeecomputersociety.org
... VLSI) digital circuits for logic **verification** and fault **...** RESQ implementation [24] for **simulating** queueing networks **... processor** sees this report, **processor** P may **...**
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[PDF] ... **verification** of a multiple-issue, pipelined, superscalar Alpha **processor**-the Alpha 21164 ...
M Kantrowitz, LM Noack - Digital Technical Journal, 1995 - linux-mips.org
... model (the X-box) to **simulate** transactions on **...** During the Alpha 21164 CPU **verification** effort, more than **...** CHECK **REGISTER** FILE TRACE COMPARE **MEMORY** STATE COMPARE **...**
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[PDF] Industrial Experience with TesU Generation Languages for P **Verification** - cadal.cse.nsysu.edu.tw
... to the cache lines accessed hy the first **processor**. **...** As a result, no hugs escaped the **verification** phase to **... test** templates takes 90 days to **simulate**, while the **...**
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How to **share memory** in a distributed system- *psu.edu [PDF]
E Upfal, A Wigderson - Journal of the ACM (JACM), 1987 - portal.acm.org
... General Terms: Algorithms, Theory, **Verification** Additional Key Words **...** the Ultracomputer, instead of **simulating** each of **...** of generality, that each **processor** of the **...**
Cited by 144 - Related articles - All 24 versions

[PDF] *Functional **verification** of the HP PA 8000 **processor**
ST Mangelsdorf, RP Gratias, RM Blumberg, R ... - Hewlett Packard Journal, 1997 - Citeseer
... cycles, with no attempt to **simulate** intermediate timing **...** still very useful because our **verification test** suites are **...** of **memory** and the **processor's** registers, and **...**
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[PDF] *Dynamic **verification** of **memory** consistency in cache-coherent multithreaded computer ...
A Meixner, DJ Sorin - Proceedings of the International Conference on ..., 2006 - Citeseer
... 2 we devise a framework that breaks the **verification** pro- **...** shown in Figure 1). First, **memory** operations are **...** program order (< p) and executed by the **processor**. **...**
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... **verification** of system-on-chip integrated circuit designs including an embedded **processor**
RJ Devins, ME Kautzman, KA Mahler, DW ... - US Patent 6,427,224, 2002 - Google Patents
... Typically, **verification** of a SOC which includes an embedded **processor** core involves using a simulator to **simulate** software models of the **processor** and a **...**
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1. Generating concurrent **test**-programs with collisions for multi ...

processor verification. Collisions occur when different processes **access** a **shared** resource. ... **memory** also define a **shared memory** model that relaxes the sim- ..... The **test** in Table 2 includes a Write-Write **True Sharing** collision of two processes. .... from **memory** 1000 to **register** R2, the **Simulate** method will up- ...
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2. Challenges in Post-silicon **Verification** of IBM's Cell/B.E. and ...

the complexity of the **test** stream generation for **processor verification** especially in a stress .... pre-allocation of resources in **registers**, **memory** ...
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3. System and method for pseudo-random **test** pattern **memory** allocation ...

In addition, the page table **memory** is allocated using a \"**true**\" **sharing** ..... **Test** pattern simulator 510 continues to **simulate** the **test** pattern and use .... A determination is made as to whether to continue **processor verification** at decision 790. .... Even so, the **processor memory** and **registers** still result in the ...
www.patentstorm.us/patents/7584394/description.html - Similar

4. Method and apparatus for creating a multiprocessor **verification** ...

Each **processor tests** consistency of data read by it, with data written by it. ... 1 is a block diagram of a cache-coherent **shared memory** multiprocessor ..... In stand-alone mode, the shadow **memory** is used to **simulate** the rest of the system. ... If the **test** case contains **true sharing**, the result will be correct but ...
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5. Missing the **Memory** Wall: The Case for **Processor**/**Memory** Integration

access all **memory** just like the **processor**. Due to the tight integra- ... Chip **verification** operation: comparestwo logic cir- cuits and **tests** them for

logIcat identity, ... tional FLC in a **shared memory** system. To **simulate** the proposed integrated ... **true sharing** misses dominate. As each molecule is described by a ...
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by A Saulsbury - 1996 - Cited by 186 - Related articles

6. Analysis of Cache-Coherence Bottlenecks with Hybrid Hardware ...

The instrumentation intercepts **memory access** instructions and ..... another **processor** in **shared** state. The remote reference is invalidated while ..... invalidation as a **true-sharing** invalidation. Otherwise, we classify the invali- ..... Execution-driven approaches are popular for **simulating memory** accesses. ...
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by J Marathe - 2006 - Cited by 3 - Related articles

7. Wisconsin Multiscalar

Transmission of cache lines in cache-coherent **shared memory** machines is necessary for .... We **simulate** an implementation of DDMT on top of a **simultaneous** .... The **processor** can use DVI to track dead **registers** and dynamically eliminate unnecessary ..... In addition, **verification** of the predicted effective address is ...
pages.cs.wisc.edu/~mscalar/abstracts.html - Cached - Similar

8. Architecture - bdc: Brian D. Carlstrom, Ph.D.

DSP **processor** with custom hw/sw - The Task of the Computer Designer computer ..... Instruction **memory access** and buffering (See also trace caches in Chapter ... FP **register** file to allow FP load/store with **simultaneous** FP ALU operation need ..... of Symmetric **Shared-Memory** Multiprocessors 560 sharing **true sharing** ...
carlstrom.com/stanford/quals/arch.txt - Cached - Similar

9. [PDF] RECAP: VIRTUAL **MEMORY** AND CACHE

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In **shared memory** programs a thread can **access** any ..... fall within a cache line: not a **true sharing**, but false ..... bez **register**, Enter_CS pause (delay). /* Can be **simulated** as a timed loop ... other **processor** suffers a miss on the load in **Test** loop; ..... **verification**) and hardware (associative lookup logic in ...
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10. Weaves: A Framework for Reconfigurable Programming

general and hence applicable to a wide variety of **shared memory** parallel ... a single framework, enabling testing of **simulated** state-machines ... direct code execution environment (DCEE) eliminates the **verification** and ..... 3D Discrete Ordinates Equation on a Massively Parallel **Processor**, Trans. Am. Nucl. ...
www.springerlink.com/index/U4591506X665N755.pdf - Similar
by J Mukherjee - 2005 - Cited by 9 - Related articles - All 4 versions

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[PDF]
M Katrowitz, LM Noack - Proceedings of the 33rd annual conference on Design ..., 1996 - portal.acm.org
... system environment, including not only the CPU chip, but **...** for tracking which registers were **unpredictable** at any **...** used by the DECchip 21164 **verification** effort. **...**
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... model (the X-box) to **simulate** transactions on **...** for tracking which registers were **unpredictable** at any **...** During the Alpha 21164 CPU **verification** effort, more than **...**
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Method for enhanced functional **testing** of a **processor** using dynamic trap handlers
RC Brockmann, K Brummel - US Patent 5,784,550, 1998 - Google Patents
... conditions that may be either **verification** of processors using a random code generator ^tabk or **unpredictable** in nature **...** JU instance, by a paraUel **processor** & a **...**
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Microprocessor **test** and **test** tool methodology for the 500 MHz IBM S/390 G5 chip
M Kusko, B Robbins, T Snethen, P Song, T ... - Proc. IEEE ITC, 1998 - doi.ieeecomputersociety.org
... The S/390 CMOS Central **Processor** (CP) is a **...** There were very few **verification** escapes - for example, the **...** feedback loops which would cause **unpredictable** results. **...**
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... , METHOD AND SOFTWARE APPLICATION FOR THE GENERATION OF **VERIFICATION** ...
JH Robinson, 2008 - freepatentsonline.com
... change of a prior state of the CPU to modify **...** instruction may be written to the **verification** program. **...** the status of the instruction is **unpredictable**, the status **...**
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H Au-ping, 2003 - ethesys.lib.fcu.edu.tw
... Implementation of MIPS-like CPU and Its Relative **Verification** Environment **...** Because a virtual prototype incorporate designers' logic **simulate**, **...**
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WC Carter, WH Joyner Jr, D Brand - Proceedings of the 16th Conference on Design ..., 1979 - portal.acm.org
... which is specified to be **unpredictable** after some **... Verification** of these microprogram controlled protocols is an **...** three processes: the CPU, the CPU- initiated I/O **...**
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M Botlo, MJ LeVine, RA Scheetz, MW Schulz, ... - IEEE Transactions on Nuclear Science, 1998 - drupal.star.bnl.gov
... These features allow the CPU to verify the **...** additional **tests** were developed for gate-level **verification**. **...** of asynchronous logic is highly **unpredictable** over the **...**
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I Wagner, V Bertacco - IEEE International Conference on Computer Design, 2008 - eecs.umich.edu
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